A True Enhancement Mode Single Supply Power HFET for Portable Applications

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ABSTRACT

A true enhancement mode heterojunction FET has been developed for low voltage, high efficiency power amplifier applications. A 12mm wide x 1.0 µm gate length device -- with no additional circuitry -- and only *a single voltage supply of 3.5V* exhibited a power output of +31.5 dBm with 75% power-added efficiency at a power gain of 11.6 dB at 850 MHz .

INTRODUCTION

For portable applications, transmit power amplifiers must operate at low voltages (≈3.5V) and be highly efficient with power added efficiencies in the mid-70% range. To date, the only devices capable of providing this type of performance were depletion mode HFETs. Unfortunately, these devices require two voltage supplies both positive and negative for operation. The negative voltage supply is realized through additional circuitry resulting in increased product cost, size and current drain. Furthermore, because of their spurious emissions, negative supplies require additional shielding which further increases product weight and cost. In addition, depletion mode FETs require a drain supply switch because their drain currents in the standby mode (IDS @ Vgs=0V) are too high (> 1µA), causing excessive degradation of battery lifetime. The device we report here requires only a single voltage supply for operation since this is a true enhancement mode device (Vth=0.5V). Additionally, because the standby current is less than 1 µA for a 12 mm wide device, a drain supply switch is not needed. Therefore this device eliminates the extra circuitry required for the negative voltage supply and drain switch which are necessary when using a depletion mode or pseudo-enhancement mode device. The device reported here is realized by further optimizing the N-channel HFET from Motorola's complementary GaAs (CGaAs^{TM}) process reported previously [1].

DEVICE & PROCESSING

The manufacturable CGaAs process reported earlier [1] [2] has been enhanced for RF integrated circuit (RFIC) applications. A schematic cross-section of the epitaxial material structure and the self-aligned ion-implanted NFET process is shown in Figure 1.

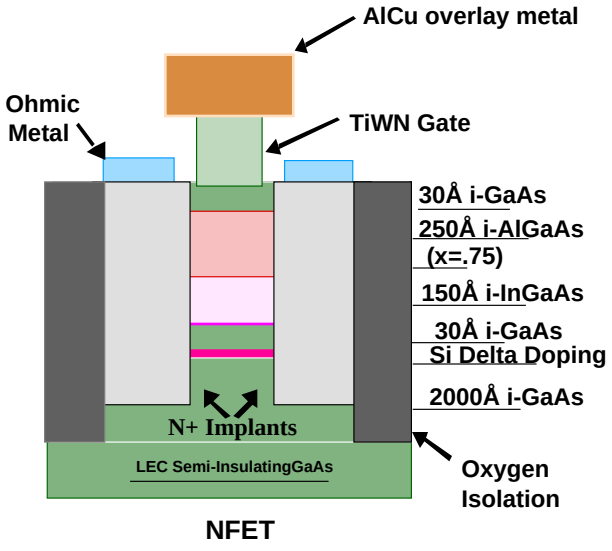

Figure 1. Cross sectional view of the enhancement mode HFET structure.

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The structure consists of 30Å GaAs cap, 250Å of undoped $Al_xGa_{1-x}As$ (x=0.75), 150Å undoped $In_yGa_{1-y}As$ (y=0.2), 2000Å undoped GaAs buffer, and LEC grown GaAs substrate. The 30Å undoped GaAs cap protects the high mole fraction AlGaAs from surface oxidation. A silicon delta doping of sheet concentration 2-6 x 10^{11} /cm^2 is incorporated 30Å away from the interface of InGaAs/GaAs for threshold voltage adjustment of the NFET device. The threshold voltages of the NFET depend on the N-Schottky barrier height, the band discontinuity of the AlGaAs/InGaAs respectively, and the delta doping concentration. The gate metal is RF reactively sputtered TiWN 4000Å thick. Next, after photo and reactive ion etch definition of the gates using a low damage SF6/CHF3/He plasma, the wafers are immediately capped with PECVD SiN to prevent oxidation of AlGaAs. Source and drain lithography and silicon implants are sequentially performed. A sidewall-assisted LDD implant process is utilized.

The wafers are then rapid thermal annealed near 800°C. Following the high temperature anneal, the devices are next isolated by oxygen implantation. Devices are subsequently capped with PECVD SiO2. Refractory ohmic contacts are next formed by dielectric assisted lift-off process and annealed. The refractory ohmics are stable in the temperature range 500°C to 600°C, which allows the ohmic metal to be interfaced with VLSI Al interconnect metalization, where Al-Cu deposition by sputtered deposition is performed near 500°C.

The rest of the processing is similar to standard Si CMOS or Si bipolar technology, consisting of TEOS deposition for further protection of the sidewalls of the gate, defining gate vias, and forming TiW/Al-Cu/TiW first metal. The first metal is also used to form T-shape gates to reduce the overall gate resistance. A TEOS interlevel dielectric is deposited and vias formed, and Al-Cu/TiW second metal added. To improve the surface topology after the metal 1 process, planarization is done at the metal 1-to-metal 2 interlevel dielectric step.

Passive circuit components, such as Si_3N_4 MIM capacitors and spiral inductors, are a new addition to the process and are formed using a process identical to Motorola's standard RF backend process, where Si_3N_4 forms the MIM capacitor dielectric between the second and third metal layers. The third metal consists of 2.5µm thick plated gold. Devices are finally passivated with SiO2 and SiN. Wafers are then thinned to the desired thickness, which is typically 100 µm, and back side metalized with gold based metal.

RESULTS

Devices from this enhanced process exhibit improved power density, efficiency and breakdown voltage. The DC characteristics of the RF version of these N-type devices are comparable to the depletion mode PHEMT, suggesting that reasonable RF performance can be expected. Statistical DC performance data for 1 µm x 12 mm devices, such as Gm, IDmax, BVgdo, and subthreshold current were measured. The mean Gm was 180 mS/mm at VDS = 3V. The mean threshold voltage (Vth) was +0.5V with a mean turn-on voltage (Vto) of +1.6V, yielding a total potential RF gate swing of 1.1V before gate-source diode turn-on. The average IDmax is around 2.2-2.4 A. The mean sub-threshold leakage current at Vds = 3V and Vgs = 0V was less than 1 µA. The mean gate to drain breakdown voltage was 12V as measured at Ig = 125 µA/mm. This is a 2X improvement in the gate to drain breakdown voltage over the original process. Further enhancements to the to improve the power density and efficiency performance of the devices continues. 12mm x 1.0 µm devices were packaged and measured on a load pull system for power output, efficiency, and gain performance at 850MHz. Figure 2 shows a plot of output power, power gain, and power-added efficiency versus input power at VDS=3.5V, IDSq=200mA. A power output of +31.5 dBm, with 75% power added efficiency and 11.6 dB of power gain were obtained at +20 dBm input power. The performance of this ***single supply*** device rivals the state-of-the-art results of depletion mode HFETs [3,4]. We believe this to be the best power and efficiency performance reported to date for an

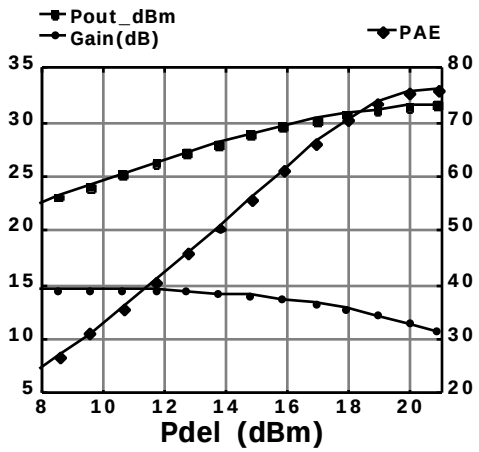

Figure 2. Output power, power gain, and power added efficiency vs. input power at 850MHz, VDS=3.5V, and IDSq=200mA.

enhancement mode FET [5]. Figure 3 shows a plot of maximum output power, maximum power gain, and maximum power-added efficiency versus drain to source voltage at an input power of+20dBm.

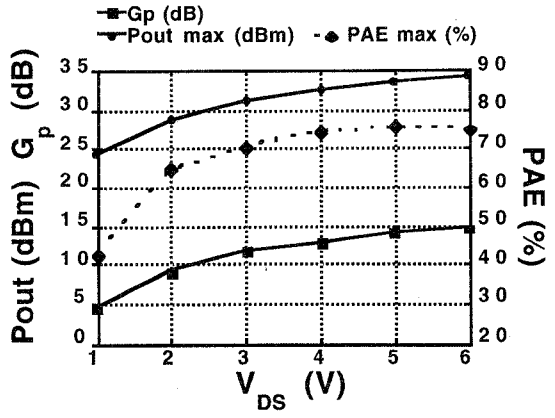

Figure 3. Maximum output power, max. power gain, and max. power-added efficiency vs. drain to source voltage, at Pin=+20dBm for a 12mm x 1.0μm device.

A two stage MMIC power amplifier was also fabricated. The power amplifier (IPA) is fully integrated except for the output matching network. The chip consists of a 3mm x 1.0μm device driving a 12mm x 1.0μm device. At VDS=3.4V and IDSq=200mA, an output power of +30.5 dBm and 59% power added efficiency with 25.5 dB power gain was achieved. Figure 4 shows a photograph of the IPA die. Power output, power added efficiency, and power gain for the IPA versus input power at 1100MHz are shown in Figure 5. This amplifier was also evaluated for ruggedness performance and was operated into a mismatch greater than a 20:1 VSWR with no degradation in performance.

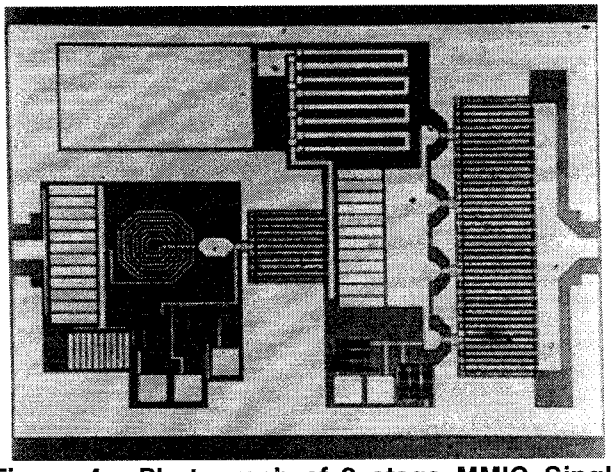

Figure 4. Photograph of 2 stage MMIC Single Supply Power Amplifier

These newly enhanced CGaAs/RF devices were also evaluated for their linearity performance for digitally modulated applications. A 12mm x 0.7μm device was packaged and measured on a load pull system at 1900 MHz using π/4QPSK modulation format. Figure 6a shows a plot of the power output, efficiency and power gain performance versus input power for a 12mm x 0.7μm device. At 1900MHz, VDS=3.5V and IDSq=100mA, the device exhibited +30 dBm output power, 50% power added efficiency, and 10 dB of power gain at a +20 dBm input power level. The corresponding adjacent channel power (ACP) was lower than 30dBc and alternate ACP was lower than 45dBc. ACP performance versus input power is shown in Figure 6b.

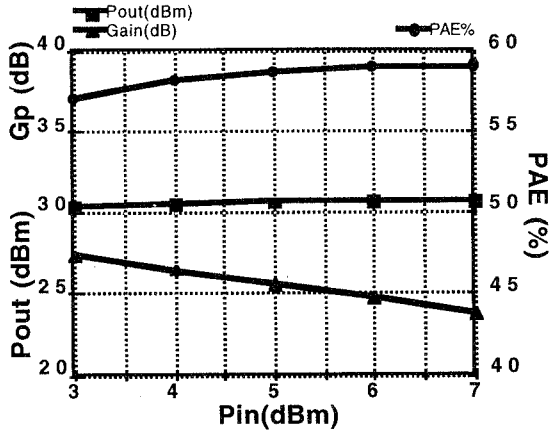

Figure 5. Plot of Pout, PAE, and Power Gain vs. input power for 2 stage MMIC Single Supply Power Amplifier.

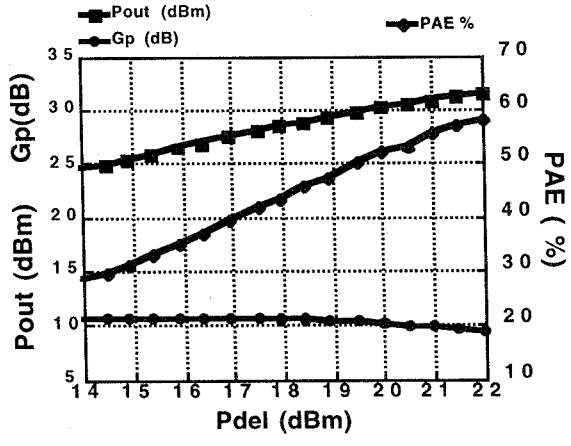

Figure 6a. Plot of Pout, PAE, and Power Gain vs. input power for a 12mm x 0.7μm device.

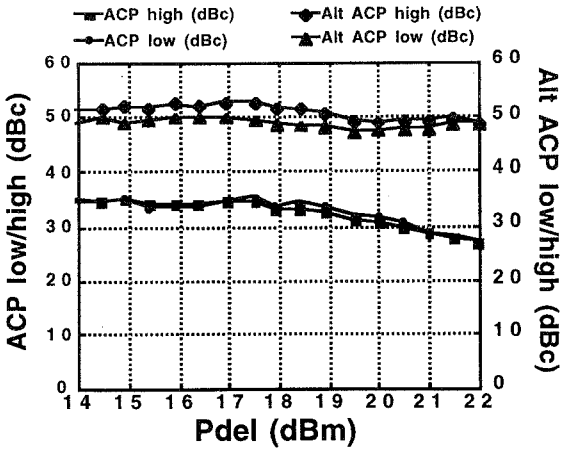

Figure 6b. Plot of ACP and Alt ACP for a 12mm x 0.7μm device vs. input power.

CONCLUSIONS

N-type FET devices from Motorola's newly enhanced complementary GaAs process (CGaAs™)/RF have demonstrated true enhancement mode, state-of-the-art performance for portable applications. The CGaAs/RF technology exceeds the demanding specifications for both 850MHz analog cellular and 1900MHz PCS/PDC applications. This process flow is now capable of building high performance RF transmitter and receiver circuits on the same process as high performance VLSI circuits.

ACKNOWLEDGEMENTS

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CGaAs™ is a trademark of Motorola Inc.

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